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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/673,953	12/21/2000	Atsushi Ito	Q60755	8878

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/673,953	ITO ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-57* is/are pending in the application.

4a) Of the above claim(s) *33-47 and 55-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-32 and 48-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/04,08/04,10/04,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I (claims 21-32, 48-54) in the reply filed on 10/01/2004 is acknowledged. The traversal is on the ground(s) that: 1) wrong standard was applied for the present application i.e. Restriction standard instead "Unity of invention" for this national stage application under 35 USC §371; and 2) restriction requirement has not established an undue burden on Examiner because Examiner has already examiner all claims before (i.e. office action of Dec. 24, 2003 and Mar. 13, 2003). This is not found persuasive because unity of invention standard does applied according to PCT rule 13.1 and 13.2, see page 2 of the Office action mailed on 09/01/2004, which states: inter alia,

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

1) Wafer Prober of Group I, wherein ceramic substrate comprises at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics. Wafer Prober of Group II does not require ceramic substrate comprises at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

2) Wafer Prober of Group II, wherein one conductor layer formed inside ceramic substrate. Wafer Prober of Group I does not require one conductor layer formed inside ceramic substrate.

Group I and Group II have different technical features as mentioned above.

Applicant failed to response, above mentioned reasoning.

Regarding other argument: 1) because claims were amended in the present RCE; and 2) because of different inventions, as mentioned above does not form single general inventive concept that require same search, they are different inventions.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-23, 25, 27-32, 48-50, 52 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tarzwell (US 4161692) in view of Leas et al. (US 5600257) and further in view of Nagasaki et al. (US 5886863).

Regarding claims 21-22 and 48-49, Trazwell in fig. 1-4 discloses a wafer prober [2] for probing a semiconductor wafer [see abstract] comprising:

a ceramic substrate [16 and lines 21-22 of column 6] and

a conductor layer [18 and 20-21] formed on a surface of said ceramic substrate, said conductor layer directly contacting a surface of the semiconductor wafer [lines 11-13 of column 5] during a probing of the semiconductor wafers [lines 11-13 of column 5].

Trazwell discloses all the elements except for said ceramic substrate comprises at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics. However, Trazwell is silent here. Leas et al. (hereafter Leas) in fig. 7b discloses a carrier 190 formed of aluminum nitride [a ceramic, see lines 29-45 of column 5, particularly lines 26-27] to test wafers [see lines 18-30 of column 11, particularly lines 26-30, and lines 32-36 of column 2]. It would have been obvious to person having ordinary skill in the art at the time the invention was made to modify ceramic substrate of Trazwell with aluminum nitride (nitride ceramic), in order to obtain low thermal coefficient of expansion (TCE) during testing of wafers.

Trazwell and Leas discloses all the elements except for said ceramic substrate is equipped with a temperature control means (Regarding claim 22). Nagasaki et al. (hereafter Nagasaki) in fig. 12a-b also discloses a wafer prober [301,302] for probing a semiconductor wafer comprising: a ceramic substrate [301], said ceramic substrate comprises at least one selected from the group consisting of nitride ceramics [lines 5-9 of column 23], carbide ceramics and oxide ceramics, and is equipped with a temperature control means [307]; and a conductor layer [302 and lines 51-56 of column 22] formed on a surface of said ceramic substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the combination of Trazwell and Leas to include temperature control means as taught by Nagasaki to the ceramic substrate, for uniformly heating the wafer through the heating of the ceramic substrate (wafer support member) [see lines 41-52 of column 25].

Regarding claims 23 and 50, Nagasaki discloses said temperature control means is a heating element [307].

~~Claims 24 and 51 (Previously Presented): The wafer prober according to Claim 21, wherein said ceramic substrate is equipped with a Peltier device~~.

Regarding claims 25 and 52, Nagasaki discloses channels are formed on said surface of said ceramic substrate [gap between 302 or channels for 307 or 306].

~~Claim 26 and 53 (Previously Presented): The wafer prober according to Claim 25, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes~~.

Regarding claim 27, Tarzwell discloses conductor layer is a chuck top conductor layer [18, 20-21].

Regarding claim 28, Nagasaki discloses said conductor layer has a thickness of 1 to 20 μm [lines 41-48 of column 5 and lines 44-53 of column 23].

Regarding claim 29, Nagasaki discloses a noble metal layer is formed on said surface of said conductor layer [lines 54-61 of column 23].

Regarding claims 30 and 54, Nagasaki discloses said conductor layer comprises nickel (porous material for claim 54) [lines 9-16 of column 9, Kovar and lines 54-57 of column 23].

Regarding claim 31, Nagasaki discloses said conductor layer comprises a titanium layer, a molybdenum layer and a nickel layer in this order [lines 1-5 of column 18].

Regarding claim 32, Tarzwell discloses wafer prober performs the probing of the semiconductor wafer by pressing a probe card on the wafer and applying an electric voltage to the semiconductor wafer [lines 11-22 of column 5].

Claims 24, 26, 51 and 53 rejected under 35 U.S.C. 103(a) as being unpatentable over Tarzwell, Leas and Nagasaki as applied to claims 25, 21 and 52, 48 above, and further in view of Zehnpfenning et al. (US 4385438).

Regarding claims 24 and 51, Tarzwell, Leas and Nagasaki discloses all the elements except for ceramic substrate is equipped with a Peltier device. However, Nagasaki discloses heating element 307. Zehnpfenning et al, (hereafter Zehnpfenning) discloses said Peltier device (lines 40-44 of column 6, also see US 3037064., and 3037065 for peltier device) to provide heating and cooling to the wafer or platen 12c to which it is embedded. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to include peltier device of Zehnpfenning with wafer prober of Tarzwell, Leas and Nagasaki, in order to control the thermal expansion of the platen or wafer.

Regarding claims 26 and 53, Tarzwell, Leas and Nagasaki discloses all the elements except for air suction holes . However, Nagasaki is silent about said channels formed on said surface of said ceramic substrate are provided with air suction holes. However, Nagasaki at lines 66-67 of column 1 and 1-2 of column 2 discloses use of vacuum chuck as wafer support member. Also, it is known in the art that vacuum chuck has air suction holes to hold the wafer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use vacuum chuck of Nagasaki with suction holes to hold the wafer during testing or other processes during manufacturing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 572-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel
December 04, 2004